VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination: 2018-19
M.Tech in VLSI Design & Embedded Systems (EVE)
Choice Based Credit System (CBCS)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4
2	PCC	18EVE12	ASIC Design	04	--	03	40	60	100	4
3	PCC	18EVE13	Advanced Embedded System	04	--	03	40	60	100	4
4	PCC	18EVE14	VLSI Testing	04	--	03	40	60	100	4
5	PCC	18EVE15	Digital VLSI Design	04	--	03	40	60	100	4
6	PCC	18EVEL16	VLSI & ES Lab-1	-	04	03	40	60	100	2
7	PCC	18RMI17	Research Methodology and IPR	02	--	03	40	60	100	2
			TOTAL	**22**	**04**	**21**	**280**	**420**	**700**	**24**

Note:- PCC: Professional Core Course

Internship: All the students shall undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.

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II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18EVE21	Design of Analog and Mixed mode VLSI Circuits	04	--	03	40	60	100	4
2	PCC	18EVE22	Real Time Operating System	04	--	03	40	60	100	4
3	PCC	18EVE23	System Verilog	04	--	03	40	60	100	4
4	PEC	18XXX24X	Professional Elective 1	04	--	03	40	60	100	4
5	PEC	18XXX25X	Professional Elective 2	04	--	03	40	60	100	4
6	PCC	18EVEL26	VLSI & ES Lab-2	--	04	03	40	60	100	2
7	PCC	18EVE27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				**20**	**06**	**18**	**340**	**360**	**700**	**24**

Note:- PCC: Professional Core Course, PEC: Professional Elective Course

Professional Elective 1		Professional Elective 2	
Course Code Under 18XXX24X	**Course Title**	**Course Code Under 18XXX25X**	**Course Title**
18EVE241	Advances in VLSI Design	18EVE251	Low Power VLSI Design
18EVE242	Nanoelectronics	18EVE252	SoC Design
18EVE243	Static Timing Analysis	18ELD253	Micro Electro Mechanical Systems

Note:

1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide in any and a senior faculty of the department. Participation in seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory.

The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

2. Internship: All the students shall undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.

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III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18EVE31	CAD of Digital Systems	04	--	03	40	60	100	4
2	PEC	18XXX32X	Professional Elective 3	04	--	03	40	60	100	4
3	PEC	18XXX33X	Professional Elective 4	04	--	03	40	60	100	4
4	Proj	18EVE34	Evaluation of Project Phase -1	--	02	--	100	--	100	2
5	INT	18EVE35	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				**12**	**02**	**12**	**260**	**240**	**500**	**20**

Note:- PCC: Professional Core Course, PEC: Professional Elective Course, Proj: Project, INT: Internship

Professional Elective 3		**Professional Elective 4**	
Course Code Under 18XXX32X	**Course Title**	**Course Code Under 18XXX33X**	**Course Title**
18ECS321	Advances in Image Processing	18EVE331	VLSI for Signal Processing
18EVE322	CMOS RF Circuit Design	18ESP332	Pattern Recognition & Machine Learning
18EVE323	Embedded Linux System Design And Development	18ECS333	Internet of Things

Note:

1. Project Phase-1: Students in consultation with the guide/co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE (University examination) shall be as per the University norms.

2. Internship: Those, who have not pursued /completed the internship shall be declared as failed and have to complete during subsequent University examinations after satisfy the internship requirements.

Internship SEE (University examination) shall be as per the University norms.

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IV SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
1	Proj	18EVE41	Project Work Phase -2	--	04	03	40	60	100	20
			TOTAL	--	**04**	**03**	**40**	**60**	**100**	**20**

Note: Proj: Project.

Note:

1. Project Phase-2:

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any and a Senior faculty of the department. The CIE marks awarded for Project Work Phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

M.Tech-VLSI & ES-2018- FIRST SEMESTER SYLLABUS

ADVANCED ENGINEERING MATHEMATICS [As per Choice Based Credit System (CBCS) Scheme] SEMESTER – I			
Course Code	**18ELD11**	**CIE**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- To learn principles of advanced engineering mathematics through linear algebra and calculus of variations.
- To understand probability theory and random process that serve as an essential tool for applications of electronics and communication engineering sciences

Modules	**(RBT) Level**
Module -1	
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples (Text Book:1).	**L1,L2**
Module -2	
Linear Algebra-II Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text. Book:1).	**L1,L2**
Module -3	
Calculus of Variations : - Concept of functional- Eulers equation. Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (Text.Book:2)	**L1,L2**
Module -4	
Probability Theory:-Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions-examples. (Text Book: 3)	**L1,L2**
Module -5	

Engineering Applications on Random processes:- Classification. Stationary, WSS and ergodic random process. Auto-correlation function-properties, Gaussian random process. (Text Book: 3)	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
5. Analyze random process through parameter-dependent variables in various random processes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

ASIC DESIGN [As per Choice Based Credit System (CBCS) scheme] SEMESTER- I			
Subject Code	**18EVE12**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Explain ASIC methodologies and programmable logic cells to implement a function on IC.
- Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
- Design CAD algorithms and explain how these concepts interact in ASIC design.

Modules	(RBT) Level
Module -1	
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells**:** Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.	**L1,L2**
Module -2	
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.	**L1-L3**
Module -3	
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.	**L1-L4**
Module -4	

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	**L1-L3**
Module -5	
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	**L1-L3**

Course outcomes: After studying this course, students will be able to:
1. Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
2. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
3. Design data path elements for ASIC cell libraries and compute optimum path delay.
4. Create floor plan including partition and routing with the use of CAD algorithms.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison-Wesley Professional; 2005.

Reference Books:
1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
3. Rakesh Chadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

ADVANCED EMBEDDED SYSTEM [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Subject	**18EVE13**	**CIE**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

Modules	**(RBT) Level**
Module -1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	**L1, L2, L3**
Module -2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13).	**L1, L2, L3**
Module -3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	**L1, L2, L3**
Module -4	
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).	**L1, L2, L3**
Module -5	

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Explain the hardware software co-design and firmware design approaches.
3. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
4. Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

VLSI TESTING [As per Choice Based credit System (CBCS) Scheme SEMESTER – I			
Subject Code	**18EVE14**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn various types of faults and fault modelling.
- Comprehend the need for testing and testable design of digital circuits
- Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
- Exemplify methods for testing sequential circuits and memory testing
- Inferring testing methods using Boundary scan, Built-in self test and other advanced topics in digital circuit design.

Modules	RBT Level
Module 1	
Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. (Text 1) **Logic Simulation:** Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation. (Text 2)	L1,L2
Module 2	
Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. (Text 1) **Testable Combinational logic circuit design:** The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic.(Text 1)	L1,L2,L3
Module 3	
Testable Combinational logic circuit design: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. (Text 1) **Test generation for Sequential circuits:** Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models. (Text 1)	L1,L2,L3
Module 4	
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable	L1,L2,L3

sequential circuit design, Level Sensitive Scan Design(LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)	
Module 5	
Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. (Text 1) **Testable Memory Design:** RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs. (Text1)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyze the need for fault modeling and testing of digital circuits
2. Generate fault lists for digital circuits and compress the tests for efficiency
3. Create tests for digital memories and analyze failures in them
4. Apply boundary scan technique to validate the performance of digital circuits
5. Design built-in self tests for complex digital circuits

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Lala Parag K., Digital Circuit Testing and Testability, New York, Academic Press, 1997.
2. Abramovici M, Breuer M A and Friedman A D, “Digital Systems Testing and Testable Design”, Wiley, 1994.

Reference Books:

1. Vishwani D Agarwal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits”, Springer, 2002.
2. Wang, Wu and Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann, 2006.

DIGITAL VLSI DESIGN [As per Choice Based Credit System (CBCS) scheme] SEMESTER –I			
Subject Code	**18EVE15**	**CIE Marks**	**40**
Number of Lecture Hours/Week of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Explain VLSI Design Methodologies
- Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
- Infer state of the art Semiconductors Memory circuits.
- Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
- Illustrate VLSI and ASIC design

Modules	(RBT) Level
Module -1	
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.	**L1, L2**
Module -2	
MOS Inverters-Static Characteristics: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.	**L2, L3**
Module -3	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).	**L1, L2, L3**
Module -4	

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques,High Performance Dynamic CMOS circuits. **BiCMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.	**L1,L2, L3**
Module -5	
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. **Design for Manufacturability:** Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.	**L2, L3**

Course outcomes: After studying this course, students will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

Question Paper Pattern

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.

Reference Books:

1. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, “Modern VLSI Design: System on Silicon” Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian, “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

<table>
<tr><td colspan="4"><u>VLSI & ES Lab-1</u>
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I</td></tr>
<tr><td>Laboratory Code</td><td>18EVEL16</td><td>CIE Marks</td><td>40</td></tr>
<tr><td>Number of Lecture Hours/Week</td><td>03</td><td>SEE marks</td><td>60</td></tr>
<tr><td>Total Number of Lecture Hours</td><td>01Hr Tutorial (Instructions)+ 03 Hours Laboratory</td><td>Exam Hours</td><td>03</td></tr>
<tr><td colspan="4">CREDITS – 02</td></tr>
<tr><td colspan="4">Course objectives: This laboratory course enables students to:
• Learn Verilog Code Programming for the design of digital circuits
• Use FPGA/CPLD board and Logic Analyzer or Chipscope to verify the results.
• Learn physical design for the digital circuits
• Learn Assembly language programming for different applications using ARM- Cortex M3 Kit and Keil uVision- 4 tool.
• Learn C language programming for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool.</td></tr>
<tr><td colspan="3">Experiments</td><td>RBT Level</td></tr>
<tr><td colspan="3">Part – A: VLSI Digital Design
Experiments to be done using
1. CADENCE/SYNOPSIS/MENTOR GRAPHICS/TANNER or any other equivalent Tool
2. FPGA/CPLD Boards with Xilinx or any other equivalent</td><td></td></tr>
</table>

ASIC-Digital Design Flow I. Write Verilog Code for the following circuits and their Test Bench for verification, observe the wave technological library (constraints to be given). Do the initial timing verification with gate level simulation. 1. An inverter, Buffer, Transmission gate and basic gates 2. Flip flop - RS, D, JK, MS, T 3. 4-bit counter [Synchronous & Asynchronous counter] **Note: For the set of experiments listed above, students can make the following flow as a study:** - Core Constrained flow - Creation of I/O pad frame - Use the created I/O pad frame for Pad constrained design. - CTS flow Only for designs which have clock **FPGA DIGITAL DESIGN** ***VLSI Front End Design programs:*** Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and use pattern generator (32 channels and logic analyzer)/Chipscope pro apart from verification by simulation 1. Write Verilog code for the design of 8-bit i. Carry Ripple Adder ii. Carry Look Ahead adder iii. Carry Skip Adder 2. Write Verilog Code for 8-bit i. Array Multiplication (Signed and Unsigned) ii. Booth Multiplication (Radix-4) 3. Write Verilog code for 4/8-bit i. Magnitude Comparator ii. LFSR iii. Parity Generator iv. Universal Shift Register 4. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with and without overlap) any sequence can be specified.	L3

Part – B: Experiments to be done using ARM Cortex M3	
ARM Cortex M3 Programs - Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ARM a) Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.........+1 b) Write an Assembly language program to store data in RAM c) Write a C program to output the "Hello World" message using UART d) Write a C program to operate a buzzer using Cortex M3 e) Write a C program to display the temperature sensed using Cortex M3. f) Write a C program to control stepper motor using Cortex M3.	L1, L2, L3

Course outcomes: This laboratory course enable the students to:

1. Understand the features of CAD tool in VLSI design.
2. Design and verify the behavior of digital circuits using digital flow
3. Verify the design using a logic analyzer
4. Analyse physical design
5. Develop Assembly language programs for different applications using ARM- Cortex M3 Kit and Keil uVision-4 tool.
6. Develop C language programs for different applications using ARM- Cortex M3 Kit and Keil uVision-4 tool.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, one experiment from Part-A and One experiment from Part-B is to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the Procedure part to be made zero.

<table>
<tr><td colspan="4"><u>RESEARCH METHODOLOGY AND IPR</u>
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER –I</td></tr>
<tr><td>Course Code</td><td>18RMI17</td><td>CIE Marks</td><td>40</td></tr>
<tr><td>Number of Lecture Hours/Week</td><td>02</td><td>Exam Hours</td><td>03</td></tr>
<tr><td>Total Number of Lecture Hours</td><td>25</td><td>SEE Marks</td><td>60</td></tr>
<tr><td colspan="4">Credits - 02</td></tr>
<tr><td colspan="4">Course objectives:
To give an overview of the research methodology and explain the technique of defining a research problem
To explain the functions of the literature review in research.
To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.
To explain various research designs and their characteristics.
To explain the details of sampling designs, and also different methods of data collections.
To explain the art of interpretation and the art of writing research reports.
To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.
To discuss leading International Instruments concerning Intellectual Property Rights. ■</td></tr>
<tr><td colspan="3">Module-1</td><td>Teaching Hours/ RBT Level</td></tr>
<tr><td colspan="3">Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India. ■</td><td>05

L1, L2</td></tr>
<tr><td colspan="4">Module-2</td></tr>
<tr><td colspan="3">Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration.
Reviewing the literature: Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed. ■</td><td>05

L1, L2</td></tr>
<tr><td colspan="4">Module-3</td></tr>
</table>

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs. **Design of Sample Surveys:** Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. ■	**05** **L1, L2**
Module-4	
Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method. **Interpretation and Report Writing:** Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout. **Interpretation and Report Writing (continued):** of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. ■	**05** **L1, L2, L3, L4**
Module-5	
Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO. ■	**05** **L1, L2, L3, L4**

Course outcomes:

At the end of the course the student will be able to:

- Discuss research methodology and the technique of defining a research problem
- Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
- Explain various research designs and their characteristics.
- Explain the art of interpretation and the art of writing research reports
- Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR. ■

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

M.Tech-VLSI & ES-2018-SECOND SEMESTER SYLLABUS

DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS [**As per Choice Based credit System (CBCS) Scheme** **SEMESTER – II**			
Subject Code	**18EVE21**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Describe basic physics and operation of MOS devices.
- Exemplify single-stage and differential amplifiers and current mirrors
- Describe operational amplifiers
- Learn the design of phase-locked-loops
- Know the role of Data converters in an ever-increasing digital world.

Modules	**RBT Level**
Module 1	
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models. **Single stage Amplifier:** Basic Concepts, Common Source stage (Text 1)	L1, L2
Module 2	
Single stage Amplifier: Source follower, common-gate stage, Cascode Stage, choice of device models. **Differential Amplifiers:** Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell (Text 1)	L1,L2
Module 3	
Passive and Active Current Mirrors: Basic current mirrors, Cascode Current mirrors, Active Current mirrors. **Operational Amplifiers (part-1):** General Considerations**,** One Stage OP-Amp, Two Stage OP-Amp, Gain boosting (Text 1)	L1,L2,L3
Module 4	
Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection. **Phase Locked Loops:** Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops, Applications (Text 1)	L1,L2,L3
Module 5	
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC (Text 2)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection.
2. Design high-performance, stable operational amplifiers with the trade-offs between speed, precision and power dissipation.
3. Design and study the behaviour of phase-locked-loops for the applications.
4. Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
5. Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Second Edition, Wiley.

Reference Book:

- Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press.

REAL TIME OPERATING SYSTEM [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	**18EVE22**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable the students to:

- Introduce the fundamental concepts of Real Time Operating Systems and the real time embedded system
- Apply concepts relating to operating systems such as Scheduling techniques, Thread Safe Reentrant Functions, Dynamic priority policies.
- Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.
- Discuss Memory management concepts, Embedded system components, Debugging components and file system components.
- Study programs for multithreaded applications using suitable data structures.

Modules	RBT Level
Module 1	
Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)	L1,L2,L3
Module 2	
Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)	L1,L2,L3
Module 3	
Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software. (Text 1: Selected topics from Chap. 4,5,6,7,11)	L1,L2,L3
Module 4	
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports. (Text 1: Selected topics	L1,L2,L3

from Chap. 8,9)	
Module 5	
Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication (Text 2: Chap. 11)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
2. Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.
3. Apply priority based static and dynamic real time scheduling techniques for the given specifications.
4. Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
5. Develop programs for multithreaded applications using suitable techniques and data structure

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Sam Siewert, “Real-Time Embedded Systems and Components”, Cengage Learning India Edition, 2007.
2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, Dream Tech Press, New edition, 2010.

Reference Books:

1. James W S Liu, “Real Time System”, Pearson education, 2008.
2. Dream Tech Software Team, “Programming for Embedded Systems”, John Wiley, India Pvt. Ltd., 2008.

SYSTEM VERILOG [As per Choice Based credit System (CBCS) Scheme] SEMESTER – II			
Subject Code	**18EVE23**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand digital system verification using object oriented methods
- Learn the System Verilog language for digital system verification.
- Create/build test benches for the basic design/methodology.
- Use constrained random tests for verification
- Understand concepts of functional coverage

Modules	RBT Level
Module 1	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench. **Data Types:** Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	L1, L2
Module 2	
Procedural Statements and Routines: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Converting the test bench and design:** Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	L1,L2,L3
Module 3	
Randomization: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control, Random Number Generators.	L1,L2,L3
Module 4	
Threads and Interprocess Communication: Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.	L1,L2,L3

<table>
<tr><td colspan="2" align="center">Module 5</td></tr>
<tr><td>Functional Coverage:
Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.</td><td>L1,L2,L3</td></tr>
<tr><td colspan="2">Course Outcomes: After studying this course, students will be able to:

1. Write test benches for moderately complex digital circuits
2. Use System Verilog language
3. Appreciate functional coverage
4. Apply constrained random tests benches using System Verilog
5. Analyze a verification case and apply System Verilog to verify the design</td></tr>
<tr><td colspan="2">Question paper pattern:
• Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
• Each full question can have a maximum of 4 sub questions.
• There will be 2 full questions from each module covering all the topics of the module.
• Students will have to answer 5 full questions, selecting one full question from each module.
• The total marks will be proportionally reduced to 60 marks as SEE marks is 60.</td></tr>
<tr><td colspan="2">Text Book:
• Chris Spear, ‘System Verilog for Verification – A guide to learning the Test bench language features’, Springer Publications, 2nd Edition, 2010.</td></tr>
<tr><td colspan="2">Reference Book:
• Stuart Sutherland, Simon Davidmann, Peter Flake, “System Verilog for Design- A guide to using system verilog for Hardware design and modeling”, Springer Pulications, 2nd Edition, 2006.
• Stuart Sutherland, Simon Davidmann, Peter Flake, System Verilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modeling, Springer Science & Business Media, 15-Sep-2006</td></tr>
</table>

ADVANCES IN VLSI DESIGN [As per Choice Based credit System (CBCS) Scheme] SEMESTER – II			
Subject Code	**18EVE241**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn circuit-oriented approach towards digital design
- Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
- Infer different approaches to digital timing and clocking circuits
- Understand the impact of clock skew on the behaviour of digital synchronous circuits.
- Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories .

Modules	RBT Level
Module 1	
Implementation Strategies For Digital ICS: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	L1,L2,L3
Module 2	
Coping With Interconnect: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	L1,L2,L3
Module 3	
Timing Issues In Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Base Technique,	L1,L2,L3

Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL. d Clocking, Self Timed Circuit Design, Self-Timed Logic - An Asynchronous	
Module 4	
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design(LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)	L1,L2,L3
Module 5	
Designing Memory and Array Structures: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Dataretention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
2. Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
3. Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
4. Infer the reliability of the memory

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

- Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, ―Digital Integrated Circuits-A Design Perspective‖, PHI, 2nd Edition.

Reference Books:

1. M. Smith, ―Application Specific Integrated circuits‖, Addison Wesley, 1997 Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006.
2. H. Veendrick, ―MOS IC‗s: From Basics to ASICs, Wiley-VCH, 1992.

NANOELECTRONICS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – II			
Subject Code	**18EVE242**	**CIE**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoelectronics .
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

Modules	(RBT) Level
Module -1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).	**L1, L2**
Module -2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties(Text1)	**L1,L2,L3**
Module -3	
Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1). **Carbon Nanostructures:** Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).	**L1, L2, L3**
Module -4	

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).	**L1, L2, L3**
Module -5	
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). **Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text1).	**L1, L2, L3**

Course outcomes: After studying this course, students will be able to:

1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future tec hnologies.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

STATIC TIMING ANALYSIS [As per Choice Based Credit System (CBCS) scheme] SEMESTER –II			
Subject Code	**18EVE 243**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Understand timing analyses at various process, environment and interconnect corners.
- Apply the learnt concepts of STA to evaluate the delay of the circuits.
- Understand and analyze the signal integrity issues for the IC.
- Generate the timing analysis report using EDA tool.
- Understand verification and analyze the generated report to identify issues for the violation
- Learn different techniques to meet timing in an IC design.
- Set up the timing analysis environment and perform the timing analysis for various cases.

Modules	(RBT) Level
Module -1	
Introduction: Nanometer Designs, What is Static Timing Analysis?. Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations, **STA Concepts:** CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions .	**L1-L2**
Module -2	
Standard Cell Library: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, Timing Models - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setup and Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State-Dependent Models XOR, XNOR and Sequential Cells, Interface Timing Model for a Black	**L1**

Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage,, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and Sequential Cells, Other Noise Models, Power Dissipation Modeling, Active Power, Double Counting Clock Pin Power, Leakage Power, Other Attributes in Cell Library, Area Specification, Function Specification, SDF Condition, Characterization and Operating Conditions, What is the Process Variable, Derating using K-factors, Library Units.	
Module -3	
Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation of Extracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets. **Delay Calculation**: Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation.	**L1-L4**
Module -4	
Configuring the STA Environment: What is the STA Environment? Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge_shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example C, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Specifying Inactive Signals, Breaking Timing Arcs in Cells, Point-to-Point Specification, Path Segmentation.	**L1-L4**
Module -5	
Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip-flop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip-flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half-	**L1-L4**

Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks, Integer Multiples, Non-Integer Multiples, Phase Shifted.	

Course outcomes: After studying this course, students will be able to:

- Evaluate the delay of any given digital circuits.
- Prepare the resources to perform the static timing analysis using EDA tool
- Prepare timing constraints for the design based on the specification.
- Generate the timing analysis report using EDA tool for different checks.
- Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing

Question paper pattern:

- The students will have to answer 5 full questions, selecting one full question from each module. Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

It is suggested that the students may be asked to conduct the following experiments to award a part of CIE marks which is reserved for the Other Activities:

In the following experiments, determine the parameters such as slack, critical path, Dynamic power, leakage power, timing and area report. Also, generate Verilog netlist, SDF file and write SDC constraints after synthesis based on the particular experiment.

1. Synthesize 4 bit counter & find the required parameters at 50 MHz (Repeat using Xilinx library also).
2. Synthesize 8 bit Mux and find the required parameters at 25 MHz (Repeat using Xilinx library also).
3. Synthesize synchronous 16 bit save carry adder for 100 MHz and find the required parameters.
4. Synthesize synchronous 16 bit save carry adder for 20 MHz and find the required parameters (Repeat the experiment for 3 Vendor library, Altera library).

5. Compare the area report and timing report as per the vendor and tablet using Pi-chart or Bar chart for expt - 4
6. Synthesize 8 bit multiplier using Xilinx Defence standard / Automotive library to determine the required parameters
7. For the given UART/Traffic signal controller, synthesize using 50 MHZ clock and 100 MHZ clock. Compare the result for both the clocks and determine the required parameters.
8. Compare one of the design through ASIC synthesis and FPGA synthesis to determine the required parameters

Text Book:

J. Bhasker, R Chadha,., “Static Timing Analysis for Nanometer Designs: A Practical Approach”, Springer, 2009.

Reference Books:

1. Sridhar Gangadharan, Sanjay Churiwala, “Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)”, Springer, 2013.
2. Naresh Maheshwari and Sachin Sapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999.

LOW POWER VLSI DESIGN [As per Choice Based Credit System (CBCS) scheme] SEMESTER –II			
Subject Code	**18EVE251**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Apply State-of-the art approaches to power estimation and reduction.
- Describe the various power reduction and the power estimation methods.
- Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system
- Know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays a major role.
- Practice the low power techniques using current generation design style and process technology.

Modules	(RBT) Level
Module -1	
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis:** SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. (Text 1)	**L1, L2**
Module -2	
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Circuit:** Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage. (Text 1)	**L1, L2, L3**
Module -3	
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic (Text 1). **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network (Text 2).	**L1, L2, L3**
Module -4	

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation (Text 1). **Low power arithmetic components:** Introduction, circuit design style, adders, multipliers, division (Text 2).	**L1- L4**
Module -5	
Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM (Text 2). **Algorithm & Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis (Text 2). **Advanced Techniques**: Adiabatic computation, pass transistor, Asynchronous circuits (Text 1).	**L1-L4**

Course outcomes: After studying this course, students will be able to:

1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation based approaches and probabilistic analysis.
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Make the power design a reality by making power dimension an integral part of the desigUse practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments. n process
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.
6. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Question paper pattern:

- The students will have to answer 5 full questions, selecting one full question from each module. Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic, 1998.
2. Jan M.Rabaey, Massoud Pedram, “Low Power Design Methodologies”, Kluwer Academic, 2010.

Reference Books:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer Academic,1995.
3. A Bellamour and M I Elmasri, “Low power VLSI CMOS circuit design”, Kluwer Academic,1995.

SoC DESIGN **[As per Choice Based credit System (CBCS) Scheme** **SEMESTER – II**			
Subject Code	**18EVE252**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50** **(10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Describe the ARM processor architecture and user-level assembly language programming
- Appreciate what a high-level language (in this case, C) really needs and how those needs are met by the ARM instruction set.
- raises the issues involved in debugging systems which use embedded
- processor cores and in the production testing of board-level systems.
- Learn the concept of memory hierarchy, discussing the principles
- of memory management and caches.

Modules	**RBT Level**
Module 1	
ARM Organization and Implementation:3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. **The ARM Instruction Set :**Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL),Branch, Branch with Link and eXchange (BX, BLX),Software Interrupt (SWI),Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions,Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.	L1,L2
Module 2	
Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment. **Architectural Support for System Development:** The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware	L1,L2

system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support.	
Module 3	
ARM Processor Cores: ARM7TDMI, ARM8,ARM9TDMI, ARM10TDMI,Discussion,Example and exercises. **Memory Hierarchy:** Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.	L1,L2
Module 4	
Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit,CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises. **ARM CPU Cores:** The ARM710T, ARM720T and ARM740T, The ARM810, The Strong ARM SA-110, The ARM920T and ARM940T, The ARM946E-S and ARM966E-S, The ARM1020E, Discussion, Example and exercises.	L1,L2
Module 5	
Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364, The SA-1100 368, Examples and exercises. **The AMULET Asynchronous ARM Processors:** Self-timed design 375, AMULET1 377, AMULET2 381, AMULET2e 384,AMULET3 387, The DRACO telecommunications controller 390, A self-timed future? 396, Example and exercises.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
2. Use the concepts and methodologies employed in designing a System-on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
4. Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.
5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Steve Furber, “ARM System-On-Chip Architecture”, Addison Wesley, 2nd edition.

References Books:

1. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.
2. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann, Publishers © 2008.
3. Michael Keating, Pierre Bricaud, “Reuse Methodology Manual for System on Chip designs”, Kluwer Accademic Publishers, 2nd edition, 2008.

MICRO ELECTRO MECHANICAL SYSTEMS [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	**18ELD253**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Know an overview of microsystems, their fabrication and application areas.
- Teach working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
- Expose the students to various application areas where MEMS devices can be used.

Modules	**RBT Level**
Module 1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	L1, L2
Module 2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics. **Engineering Science for Microsystems Design and Fabrication:** Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	L1, L2
Module 3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	L1,L2,L3
Module 4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of	L1,L2,L3

Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	
Module 5	
Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micro-manufacturing. **Microsystem Design:** Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	L1,L2,L3
Course Outcomes: After studying this course, students will be able to: 1. Understand the technologies related to Micro Electro Mechanical Systems. 2. Describe the design and fabrication processes involved with MEMS devices. 3. Analyse the MEMS devices and develop suitable mathematical models 4. Understand the various application areas for MEMS devices	
Question paper pattern: • Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks. • Each full question can have a maximum of 4 sub questions. • There will be 2 full questions from each module covering all the topics of the module. • Students will have to answer 5 full questions, selecting one full question from each module. • The total marks will be proportionally reduced to 60 marks as SEE marks is 60.	
Text Book: • Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, John Wiley & Sons, 2008. ISBN: 978-0-470-08301-7	
Reference Books: 1. Hans H. Gatzen, Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015. **2.** Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Micro electromechanical Systems (MEMS), Cenage Learning.	

VLSI & ES Lab-2 [As per Choice Based Credit System (CBCS) scheme] SEMESTER – II			
Laboratory Code	**18EVEL26**	**IA Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions) + 03 Hours Laboratory**	**Exam Mark**	**60**
		Exam Hour	**03**
CREDITS – 02			

Course objectives: This course will enable students to:

- Learn the CAD tool and the flow of the Full Custom IC design cycle.
- Learn running DRC, LVS and Parasitic Extraction of the various designs.
- Create various components like inverter, differential amplifier and use the same in the design of operational amplifier, R-2R based DAC and ADC.
- Understand the suitability of different techniques of IPC and task switching in a multithreaded application.
- Study and implement different types of data structures required to implement inter task communication.
- Implement Inter task communication using an appropriate data structure.

Experiments	(RBT) Level
PART A: VLSI Design. **Experiments to be conducted using suitable CAD tool** 1. Design an **Inverter** with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Check for XX d. Extract RC and back annotate the same and verify the Design e. Verify & Optimize for Time, Power and Area to the given constraint***	**L2,L3,L4**

2.Design the following circuits with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS c. Check for XX d. Extract RC and back annotate the same and verify the Design i) Single Stage differential amplifier ii) Common source amplifier iii) Design an op-amp with given specification* using differential amplifier Common source amplifier in library** iv) Design a 4 bit R-2R based DAC for the given specification**	
3. Design an Integrator using OPAMP (First Order)	
4. Design a Differentiator using OPAMP (First Order)	
5. Design and characterize a basic Sigma delta ADC from the available designs.	
PART B: RTOS programs using C language in LINUX OS. 1. Develop programs to (a) create child process and display it's id and (b) Execute child process function using switch structure 2. Develop and test program for a multithreaded application, where communication is through a buffer for the conversion of lowercase text to uppercase text, using semaphore concept. 3. Develop and test program for a multithreaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text. 4. Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application 5. Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux. 6. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism	**L1, L2, L3**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Design, implement and analyse analog, digital and mixed mode circuits
- Learn the various issues in Mixed signal designs basically data converters.
- Acquire hands-on skills of using CAD tools in VLSI design.
- Appreciate the design process in VLSI through a mini-project on the design of a CMOS sub-system.
- Select a suitable task switching technique in a multithreaded application.
- Implement different techniques of message passing and Inter task communication.
- Implement different data structures such as pipes, queues and buffers in multithreaded programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, two questions using different tool to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

M.Tech-VLSI & ES-2018- THIRD SEMESTER SYLLABUS

CAD of DIGITAL SYSTEMS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – III			
Course Code	**18EVE31**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits –03			

Course objectives: This course will enable students to:
- Use graph theory in physical design
- Learn various optimization methods
- Understand different techniques for placement and routing

Modules	RBT Levels
Module-1	
Introduction to Design Methodologies: The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies. **VLSI Design Automation tools**: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools. **Algorithmic graph theory and computational complexity:** Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms. **Tractable and intractable problems:** Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences.	L1, L2
Module-2	
General purpose methods for combinational optimization: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods. **Layout compaction:** Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues.	L2,L3
Module-3	
Placement and partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning. **Floor planning:** Floorplanning Concepts, Shape Functions and Floorplan Sizing.	L2,L3
Module-4	

Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing. **Simulation:** General Remarks on VlSl Simulation, Gate-level Modeling and Simulation, Switch-level Modeling and Simulation.	L2,L3
Module-5	
Logic Synthesis and Verification: Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis **High level synthesis:** Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the Assignment Problem, High-level Transformations.	L3,L4

Course Outcomes: After studying this course, students will be able to:
1. Solve graph theoretic problems.
2. Evaluate the computational complexity of an algorithm
3. Write algorithms for VLSI Automation
4. Simulate and synthesize digital circuits using VLSI automation tools.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- S H Gerez, “ Algorithms for VLSI Design Automation”, Wiley, India, 2nd edition

Reference Books:
- N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”. Springer International edition, 3rd edition.

ADVANCES IN IMAGE PROCESSING [As per Choice Based credit System (CBCS) Scheme SEMESTER – III			
Subject Code	**18ECS321**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

1. Acquire fundamental knowledge in understanding the representation of the digital image and its properties
2. Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
3. Select the region of interest in the image using segmentation techniques.
4. Represent the image based on its shape and edge information.
5. Describe the objects present in the image based on its properties and structure.

Modules	RBT Level
Module 1	
The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	L1
Module 2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	L1, L2
Module 3	
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.	L1, L2, L3
Module 4	
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	L1, L2, L3
Module 5	
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and	L1, L2, L3

watersheds.

Course Outcomes: After studying this course, students will be able to:

- Understand the representation of the digital image and its properties
- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011.

CMOS RF CIRCUIT DESIGN [As per Choice Based credit System (CBCS) Scheme SEMESTER – III			
Subject Code	**18EVE322**	**IA Marks**	**40**
Number of Lecture Hours/Week	**04**	**Exam marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
- Appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
- Understand the design of RF building blocks such as Low Noise Amplifiers, Mixers, Oscillators and PLLs

Modules	RBT Level
Module 1	
Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion	L1,L2,L3
Module 2	
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.	L1,L2,L3
Module 3	
Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.	L1,L2,L3
Module 4	
Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.	L1,L2,L3
Module 5	
VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio	L1,L2,L3

frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design	

Course Outcomes: After studying this course, students will be able to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.

The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- B. Razavi, "RF Microelectronics", PHI, second edition.

Reference Books:

1.R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
2. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
3. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

EMBEDDED LINUX SYSTEM DESIGN AND DEVELOPMENT [As per Choice Based Credit System (CBCS) scheme] SEMESTER – III			
Course Code	**18EVE323**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits –03			

Course objectives: This course will enable students to:

- Understand transition roadmap from a traditional RTOS to embedded Linux.
- Explain the steps involved in building a GNU cross-platform tool chain
- Explains boot loader architecture, system memory map, both hardware and software memory maps, interrupt management, the PCI subsystem, timers, UART, and power management.
- Explains the MTD subsystem architecture for accessing flash devices, discusses various embedded file systems
- Learn various embedded drivers such as the Serial driver, Ethernet driver, I2C subsystem, and USB gadgets.

Modules	**RBT Levels**
Module-1	
Introduction: History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap. **Getting Started**: Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU Cross-Platform Tool chain.	L1, L2
Module-2	
Board Support Package: Inserting BSP in Kernel Build Procedure, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART, Power Management.	L2,L3
Module-3	
Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices, Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory.	L2,L3
Module-4	
Embedded Drivers : Linux Serial Driver, Ethernet Driver , I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules**.**	L2,L3
Module-5	
Porting Applications: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.	L2,L4

Course Outcomes: After studying this course, students will be able to:

- Understand the embedded Linux development environment.
- Understand and create Linux BSP for a hardware platform.
- Understand the Linux model for embedded storage and write drivers and applications for the same.
- Understand various embedded Linux drivers such as serial, I2C, and so on.
- Port applications to embedded Linux from a traditional RTOS.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- P.Raghvan,Amol Lad,Sriram Neelakandan, “Embedded Linux System Design And Development”, Auerbach Publications,Taylor & Francis Group, 2006 .

Reference Book:

- Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum, “Building Embedded Linux Systems” O’Reilly publications, 2nd edition.

VLSI DESIGN FOR SIGNAL PROCESSING [As per Choice Based credit System (CBCS) Scheme SEMESTER – III			
Subject Code	**18EVE331**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
- Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead.

Modules	RBT Level
Module 1	
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.	L1, L2
Module 2	
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.	L1,L2,L3
Module 3	
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Folding:** Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.	L1,L2,L3
Module 4	
Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.	L1,L2,L3
Module 5	
Pipelined and Parallel Recursive and Adaptive Filter: Pipeline	L1,L2,L3

Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.	

Course Outcomes: After studying this course, students will be able to:

1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
2. Use pipelining and parallel processing in design of high-speed /low-power applications
3. Apply unfolding in the design of parallel architecture
4. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
5. Develop an algorithm or architecture or circuit design for DSP applications

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Keshab K.Parthi, "VLSI Digital Signal Processing systems, Design and implementation ", Wiley 1999.

Reference Books:

1. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill,1994.
2. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
4. Lars Wanhammar, “DSP Integrated Circuits”, Academic Press Series in Engineering, 1st Edition.

PATTERN RECOGNITION and MACHINE LEARNING
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18ESP332**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: The objective of the course is to discusses main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems. Special emphasis will be given to regression, classification, regularization, feature selection and density estimation in supervised mode of learning.

Modules	RBT Levels
Module-1	
Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory **Distributions:** Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods. **(Ch.: 1,2)**	**L1,L2**
Module-2	
Supervised Learning **Linear Regression Models:** Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison **Classification & Linear Discriminant Analysis:** Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode **Ch. :3,4)**	**L1,L2,L3**
Module-3	
Supervised Learning **Kernels:** Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes **Support Vector Machines:** Maximum Margin Classifiers, Relevance Vector Machines **Neural Networks:** Feed-forward Network, Network Training, Error Backpropagation **(Ch:5,6,7)**	**L1,L2,L3**
Module-4	
Unsupervised Learning: **Mixture Models:** K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM. **Dimensionality Reduction:** Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models **(Ch.: 9,12)**	**L1,L2,L3**
Module-5	

Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models **(Ch.:8,13)**	**L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

1. Identify areas where Pattern Recognition and Machine Learning can offer a solution.
2. Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. Describe and model data.
4. Solve problems in Regression and Classification.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Pattern Recognition and Machine Learning. Christopher Bishop. Springer, 2006

INTERNET of THINGS
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18ECS333**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: This course will enable students to:

- Introduce concept of IOT and its applications in today's scenario.
- Understand IOT content generation and transport through networks
- Understand the devices employed for IOT data acquisition and communication access technologies
- Introduce some use cases of IOT

Module-1	RBT
What is IOT Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges **IOT Network Architecture and Design** Drivers behind new network Architectures, Comparing IOT Architectures, M2M architecture, IOT world forum standard, IOT Reference Model, Simplified IOT Architecture.	**L1, L2**
Module-2	
IOT Network Architecture and Design Core IOT Functional Stack, Layer1(Sensors and Actuators), Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IOT Network management. Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics IOT Data Management and Compute Stack	**L2,L3**
Module-3	
Engineering IOT Networks Things in IOT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks IOT Access Technologies, IEEE 802.15.4 Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat0, Cat-M, NB-IOT	**L2,L3**
Module-4	

Engineering IOT Networks IP as IOT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IOT. Application Protocols for IOT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IOT Application Layer Data and Analytics for IOT – Introduction, Structured and Unstructured data, IOT Data Analytics overview and Challenges.	**L3,L4**
Module-5	
IOT in Industry (Three Use cases) IOT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation. Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.	**L3,L4**

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic concepts IOT Architecture and devices employed.
2. Analyze the sensor data generated and map it to IOT protocol stack for transport.
3. Apply communications knowledge to facilitate transport of IOT data over various available communications media.
4. Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.

Text Book:

- CISCO, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT, Pearson Education; First edition (16 August 2017). ISBN-10: 9386873745, ISBN-13: 978-9386873743

Reference Book:

- Arshdeep Bahga and Vijay Madisetti, 'Internet of Things – A Hands on Approach', Orient Blackswan Private Limited - New Delhi; First edition (2015), ISBN-10: 8173719543, ISBN-13: 978-8173719547